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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/530,490 04/28/00 MIYAMOTO

T H-914

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EXAMINER
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GRAYBILL, D

ART UNIT	PAPER NUMBER
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2814

**DATE MAILED:**  
07/05/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

Application No.

09/530,490

Applicant(s)

MIYAMOTO ET AL.

Examiner

David E Graybill

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-19 and 30-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 and 30-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/627,008.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_

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The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-19 and 30-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the scope of the term "type" cannot be determined because the common qualities that distinguish the individual members as an identifiable class are not recited in the claims, and they cannot otherwise be determined.

The scope of claim 5 cannot be determined because the limitation "a plurality of stages of Au bumps" cannot be understood.

There is insufficient literal antecedent basis for the following:

Claim 1, "their other end portions";

Claims 1 and 7, "the principal face";

Claims 1 and 30, "their one-end portions";

Claim 3, "the side faces," and "said semiconductor chip";

Claims 4 and 21, "the upper face";

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Claim 5, "the upper faces";

Claim 30, "the principal faces thereof," and "the principal faces of said semiconductor chip forming areas," "the other end portions," and, "the oneend portions";

Claim 32, "the AU bump electrodes," and, "the surfaces of said plurality of bonding pads."

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

Claim 5 has not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claim; hence, it would not be proper to reject the claim on the basis of prior art. As stated in *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. See also MPEP 2173.06.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1, 4, 7-14, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Wojnarowski (5366906) and Schroeder (5742100).

At column 5, line 3 to column 16, last line, Wojnarowski teaches the following:

1. A semiconductor device characterized: in that an elastomer layer 18 is formed over a plurality of semiconductor elements and bonding pads 14, which are formed over a plurality of chip

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areas 12 of the principal face of a semiconductor wafer 10; and in that electrodes are electrically connected at their one-end portions with said bonding pads through through holes opened in said elastomer and at their other end portions with wires 21 arranged over said elastomer layer.

4. A semiconductor device as set forth in 1, characterized: in that said wires are formed over one face of an insulating tape 70 jointed to the upper face of said elastomer layer; and in that said wires and said bonding pads are electrically connected through the electrodes jointed over said bonding pads.

7. A semiconductor device as set forth in 1, characterized in that said elastomer layer is made of either a photosensitive resist applied to the principal face of said semiconductor wafer or a photosensitive film adhered to the principal face of said semiconductor wafer.

8. A semiconductor device as set forth in 1, characterized in that said elastomer layer has a modulus of elasticity of 1 to 5,000 MPa.

9. A semiconductor device as set forth in 1, characterized in that said elastomer layer has a modulus of elasticity of 1 to 1,000 MPa.

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10. A semiconductor device as set forth in 1, characterized in that said elastomer layer has a modulus of elasticity of about 1 to 500 MPa.

14. A semiconductor device as set forth in 1, characterized in that said bump electrodes have a spacing larger than that of said bonding pads.

16. A semiconductor device as set forth in 1, characterized in that said elastomer layer in the vicinity of said bump electrodes have slits 66.

18. A semiconductor device as set forth in 1, characterized in that the wires arranged over said elastomer layer are formed at least partially to have a plurality of wires.

Although Wojnarowski does not appear to explicitly teach the particular claimed moduli of elasticity, these limitations are an inherent property of the elastomer layer material of Wojnarowski.

In any case, it is inherent that the elastomer layer of Wojnarowski has a modulus of elasticity, and it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed moduli of elasticity because applicant has not disclosed that the moduli are for a particular unobvious purpose, produce

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an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another moduli. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

Also, Wojnarowski does not appear to explicitly teach the following:

11. A semiconductor device as set forth in 1, characterized in that said elastomer layer has a film thickness of 0.005 to 0.15 mm.

12. A semiconductor device as set forth in 1, characterized in that said elastomer layer has a film thickness of 0.01 to 0.1 mm.

13. A semiconductor device as set forth in 1, characterized in that said elastomer layer has a film thickness of 0.02 to 0.1 mm.

In any case, Wojnarowski teaches that the layer has a thickness, and it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed thickness limitations because applicant has not disclosed that the limitations are for a

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particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another thickness.

In addition, Wojnarowski does not appear to explicitly teach that the electrodes are Au bumps and that the Au bumps are sealed with a resin filled in the through holes of the elastomer layer.

Nonetheless, at column 1, line 43 to column 4, line 31, Schroeder teaches a process comprising wherein Au bumps electrodes 16 are sealed with a resin 22 filled in through holes 19 of an elastomer layer 12.

Furthermore, it would have been obvious to combine the process of Schroeder with the process of Wojnarowski because it would facilitate electrical connection.

Claims 2, 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Wojnarowski and Schroeder as applied to claims 1, 4, 7-14, 16 and 18, and further in combination with Akagawa (6121688).

The combination of Wojnarowski and Schroeder does not appear to explicitly teach the following:

2. A chip size package type semiconductor device comprising semiconductor chips obtained by dividing the chip area of said semiconductor wafer as set forth in 1.

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3. A semiconductor device as set forth in 2, characterized in that a protective layer is formed on the side faces of said semiconductor chip.

17. A semiconductor device as set forth in 1, characterized in that the wires arranged over said elastomer layer are formed at least partially to have a curved pattern.

Nevertheless, at column 4, lines 53-60; column 5, lines 30-36; and column 6, lines 9-21, Akagawa teaches these limitations.

Moreover, it would have been obvious to combine the process of Akagawa with the process of the applied prior art because it would provide wires, result in a reduction in production cost and protect the chip.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Wojnarowski and Schroeder as applied to claims 1, 4, 7-14, 16 and 18, and further in combination with Lur (5358733).

The combination of Wojnarowski and Schroeder does not appear to explicitly teach the following:

15. A semiconductor device as set forth in 1, characterized in that said elastomer layer has an undulated surface.

Notwithstanding, at column 5, lines 41-58, Lur teaches a process wherein a layer under a wire has an undulated surface.

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Furthermore, it would have been obvious to combine the process of Lur with the process of the applied prior art because it would reduce stress in the wafer and wire.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Wojnarowski and Schroeder as applied to claims 1, 4, 7-14, 16 and 18, and further in combination with Iwasaki (5892273).

The combination of Wojnarowski and Schroeder does not appear to explicitly teach the following:

19. A semiconductor device as set forth in 1, characterized: in that the wires arranged over said elastomer layer are oriented at a right angle with respect to the direction joining the bump electrodes connected with said wires and the center of said chip area: and in that the wires arranged at the peripheral edge portion of said chip area are longer than the wires arranged at the center portion of said chip area.

However, at column 11, last paragraph, Iwasaki teaches a process wherein wires 15 arranged over an elastomer layer 13 are oriented at a right angle with respect to the direction joining the electrodes 12 connected with the wires and the center of a chip 11 area: and in that wires 15 arranged at a peripheral edge portion of the chip area are longer than wires 15 arranged at a center portion of the chip area.

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In addition, it would have been obvious to combine the process of Iwasaki with the process of the applied prior art because it would provide wires.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30, 31 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Wojnarowski (5366906).

At column 5, line 3 to column 16, last line, Wojnarowski teaches the following:

30. A semiconductor device comprising: a semiconductor wafer 10 having a plurality of semiconductor chip forming areas defined by scribe lines 67 and having a plurality of semiconductor elements 12 and a plurality of bonding pads 14 formed on the principal faces thereof; an elastic insulating film 18 formed on the principal faces of said semiconductor chip forming areas and having through holes at positions corresponding to said plurality of bonding pads; a plurality of conductive layers 21 having their one-end portions thereof formed on said insulating film while the other end portions thereof are electrically

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connected to said plurality of bonding pads corresponding thereto through said through holes; and a plurality of bump electrodes 73 formed on the one-end portions of said plurality of conductive layers and electrically connected to said plurality of bonding pads corresponding thereto through said conductive layers.

31. A semiconductor device as set forth in claim 30, characterized in that a plurality of semiconductor chips are supplied by cutting said semiconductor wafer along said scribe lines.

33. A semiconductor device as set forth in claim 30, characterized in that said bump electrodes are solder bump electrodes, respectively.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski as applied to claims 30, 31 and 33, and further in combination with Akagawa (6121688).

Wojnarowski does not appear to explicitly teach the following:

32. A semiconductor device as set forth in claim 30, characterized in that said conductive layer includes the Au bump electrodes individually formed on the surfaces of said plurality of bonding pads and wiring layer formed over said Au bump electrodes.